IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Scott Derner	Examiner:	Tan Nguyen
Serial No.:	10/017,658	Group Art Unit:	2818
Filed:	December 12, 2001	Docket:	400.105US01
Title:	HALF DENSITY ROM EMBEDDED DRAM		

RESPONSE

Mail Stop Non-Fee Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Introductory Comments

In response to the Office Action dated May 21, 2003 in the above-identified patent application, please consider the following comments.

REMARKS

Rejection Under 35 U.S.C. §102

Claims 1-4, 9-12, 14-16, 17 and 21-22 were rejected under 35 U.S.C. §102(b), as being anticipated by Takasugi (U. S. Pat. No. 5,663,906). Applicant traverses this rejection, and submits that Takasugi does not contain each and every element of the claims.

Specifically, Takasugi does not, as the Office Action asserts, contain "hard programmed" ROM cells. As is clearly asserted in the Office Action, at the first full paragraph of page 3, "memory cells ... are electrically connected to *either the first conductive line ... or the second conductive line*. ... [Takasugi] inherently teaches the memory cells are hard programmed to a first data state." (emphasis added). Applicant submits that Takasugi in fact *explicitly* states that the ROM cells are not hard programmed. In fact, they are clearly soft programmed because they are electrically coupled, non-permanently, to one of the two conductive lines. The present

claims, in contrast, require hard programming to one data state. As is discussed in the specification, "hard programming" is a permanent state of the cells that are hard programmed. That state is created by eliminating cell dielectric, forming an electrical plug, anti-fuse programming, creation of a high leakage path such as through an active area to the substrate, or shorting the cell to a word line. Each of these hard programming is a permanent solution that is performed during fabrication. In contrast, the Takasugi reference, as has been discussed above, allows for the electrical connection after fabrication of the cells to a changeable potential. This is clearly not "hard programming" as is described in the specification of the present application. The language of the claims should be interpreted in light of the specification. Fro the specification of the present application, it is clear that the hard programming of the claims is a permanent type of programming, not the transient programming of Takasugi. As such, since claims 1, 9, 14, and 17 all recite "hard programming," the claims define over Takasugi, which does not contain such hard programming.

Still further, claim 14 recites "a half-density read only memory" as well as "hard programming." Each of the memory cells in Takasugi is described as its own individual data cell. This is not true in the case of a half-density memory, in which two cells are used for each datum.

Claims 2-4, 8, 10-13, 15-16, and 21-22 depend from and further define patentably distinct claims 1, 9, 14, or 17 and are also believed allowable.

Rejections Under U.S.C. § 103

Claims 8 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takasugi in view of Koga (U. S. Patent No. 5,675,547). Applicant traverses this rejection. As has been mentioned, claims 8 and 13 depend from and further define patentably distinct claims 1, and 9 respectively and are also believed allowable.

Further, the disclosure of Takasugi already contains a disclosure of creating transient programming of ROM cells, and spends a great deal of disclosure outlining no less than 21 embodiments, each of which contains the same type of transient programming. Koga on the other hand, creates ROM cells by destroying an insulating layer. There is no need for Takasugi

to take such a step, and indeed Koga teaches away from the teachings of Takasugi, since stated objects of Takasugi are to "provide a semiconductor memory device having high flexibility, which is capable of having to ratio between a volatile memory cell section easily determined and a non-volatile section according to a user's demand" as well as "to provide a semiconductor memory device wherein volatile memory cells and non-volatile memory cells can be easily and inexpensively constructed within a single memory cell array." The processes of Koga, which add steps and complexity to violate the first above-mentioned object, also violate the second above-mentioned object by creating a memory that does not contain any flexibility of volatile to non-volatile memory cell ratio according to a user's demand. As such, modifying Takasugi with the teachings of Koga would both change the principle of operation of Takasugi by making it inflexible and more complex, and would render Takasugi unsatisfactory for its intended purpose of providing a flexible, user determined volatile to non-volatile memory cell ratio memory array. These changes are in violation of the requirements of MPEP 2143.01, which states in pertinent part:

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) ... If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

As such, it is improper to combine Takasugi and Koga, and Applicant respectfully requests that the rejection under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the above amendment and response, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicant's representative at direct dial (612) 312-2203 if there are any questions regarding this response or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 21 August 2003

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TRANSMITTAL FORM UNDER 37 CFR 1.10
(LARGE ENTITY)

Title: HALF DENSITY ROM EMBEDDED DRAM

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Enclosures

The following documents are enclosed:

X A Response to Office Action (4 pgs.)

X A return postcard.

Please charge any additional fees or credit any overpayments to Deposit Account No. 501373.

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Fee Calculation

	Number of Claims		Prv. Amt.	Extra Claims		Fee		Fee Paid
Total Claims		-20		0	X	$18	=	
Independent Claims		-3		0	X	$84	=	
							=	
							Total	

Submitted By

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Signature				Date	August 21, 2003

Certificate of Mailing

"Express Mail" mailing label number: EV256356907US Date of Deposit: August 21, 2003
These papers and fees are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and addressed to the Mail Stop Non-Fee Amendment, Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450.